REMARKS

Claims 36-39 were presented for examination and have been amended. Claims 36-39 are presently pending before the Examiner. Further examination and reconsideration are respectfully requested in view of the amendments and remarks made in this Response.

The Examiner required that a new title, clearly indicative of the claimed invention, be supplied. Accordingly, the title has been amended to clearly indicate the invention to which the claims are directed.

The Examiner indicated that the current status of the cross-referenced patent applications should be added to the specification. Accordingly, the specification has been amended to indicate the current status of the cross-referenced patent applications.

Claims 36 and 38-39

Claims 36 and 38-39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Margulis *et al.* (U.S. Patent 4,581,990; hereinafter "Margulis") in view of Johnson *et al.* (U.S. Patent 4,581,990; hereinafter "Johnson") or Manning (U.S. Patent 5,610,864; hereinafter "Manning").

Margulis shows a selection between a burst mode and a page mode for an asynchronous DRAM. (*See,* Margulis, figures 1 and 2.) The Examiner states, and Applicants agree, that Margulis does not specifically disclose a pipelined mode.

The Examiner contends that Johnson discloses the concept of selecting between a burst mode and a pipelined mode of operation, referring to Johnson at figures 5 and 6, and at column 10, lines 48-49. Applicants respectfully traverse this contention.

Johnson discloses a RISC processor 101 connected to a data store 103 via shared address bus 111 and data bus 120. (*See*, Johnson, FIG. 1.) The "interface," provided by three separate buses (*see,* Johnson, col.2, lines 38-46), is synchronous (*see,* Johnson, col.8, lines 28-31). In Johnson, an inquiry is made to determine if a memory supports a burst mode or a pipelined mode. (*See*, Johnson, col. 10, lines 48-65.)

It is Applicants' position that Johnson does not describe or show a memory having both burst and pipelined modes; rather, Johnson describes that an inquiry is to be made to determine which type of memory architecture is used, namely, burst or pipelined.

The Examiner contends that Manning discloses mode circuitry configured to select between two modes, referring to Manning at figure 1, column 5, lines 41-50, and column 6, lines 14-16. Manning discloses an asynchronous DRAM having dual modes of operation, namely, burst and EDO page mode (Manning, col. 6, lines 22-26); standard fast page mode and burst mode (Manning, col. 7, lines 43-48); and fast page mode, EDO page mode, static column mode and burst operation (Manning, col. 7, lines 49-54).

Though Manning does discuss pipelined architectures (*see,* Manning, col.5, lines 43-50), Manning does not describe or show a memory having both a pipelined architecture and a burst architecture.

By way of example and not limitation, Claim 36, as amended, recites in relevant part: "...selecting between a burst mode and a pipelined mode of operation of the asynchronously-accessible dynamic random access memory..." Claim 36 recites an asynchronously-accessible DRAM having both burst and pipelined modes of operation. Margulis and Johnson or Manning take singly or in any combination do not describe or show an asynchronously-accessible DRAM having both burst and pipelined modes of operation.

Furthermore, it is Applicants' position that Johnson does not describe an asynchronous operating environment. In each timing diagram in Johnson, a system clock signal ("SYS CLK" or "SYSCLK") is shown along with the *IRDY signal and the *IRDY signal is synchronized to the SYSCLK signal. The asynchronously-accessible memory of Margulis is a distinctly different system than the synchronous memory interface of Johnson. Accordingly, it is Applicants' position that there is no suggestion to combine Margulis and Johnson, and that the combination of Margulis and Johnson is improper hindsight reconstruction in view of the present invention.

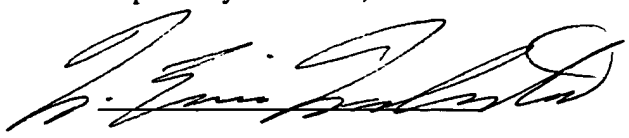
For each of the above independent reasons, it is respectfully submitted that independent Claim 36 is not rendered obvious by the combination of Margulis with Johnson or Manning. Accordingly, it is respectfully submitted that Claim 36 is allowable over the cited art. Claims 38 and 39 are dependent on an allowable base claim, and thus are likewise allowable.

Claim 37

Claim 37 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Margulis in view of Johnson *et al.* or Manning and further in view of the "1995 DRAM Data Book " of Micron Technology, Inc. at pages 4-1 to 4-42. The aforementioned remarks with respect to Claims 36 and 38-39 are hereby incorporated by reference with respect to the rejection of Claim 37. Accordingly, Claim 37 is dependent on an allowable base claim, and thus is likewise allowable.

It is believe that Claims 36-39 are allowable over the cited reference for the above-stated reasons. As it is believed that the application is in condition for allowance, such allowance is earnestly solicited.

Respectfully submitted,



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